Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus having a CPU ~~and a bridge controller~~ wherein the improvement comprises:

a clock generator generating a first clock signal for the CPU ~~operating in one of AC power mode or battery power mode~~, and a second clock signal ~~for the bridge controller~~, ~~operating in one of AC power mode or battery power mode,~~ wherein the first and second clock signals are two distinct clock signals outputted by the clock generator and have different frequencies; and

a bridge controller comprising a logic device for adjusting the second clock signal based on a power source and independent of the first clock signal.

2. (Currently Amended) The apparatus of claim 1, wherein the bridge controller controls a clock speed of a bus for data communication among a plurality of peripheral devices of the ~~portable device~~apparatus.

3. (Currently Amended) The apparatus of claim 1, wherein the ~~improvement further comprises a first phase locked loop (PLL) receiving the first clock signal for the CPU and~~

~~adjusting the first clock signal based on~~power source is one of AC power mode and battery power mode.

4. (Cancelled)

5. (Currently Amended) The apparatus of claim 1, wherein the ~~portable device~~apparatus further includes a video processor and the clock generator generates a third clock signal for the video processor, the third clock signal being distinct from the first and second clock signals and having a different frequency than the first and second clock signals.

6. (Currently Amended) The apparatus of claim 5, wherein the improvement further comprises a ~~third phase locked loop (PLL)~~second logic device for receiving the third clock signal and adjusting the third clock signal based on ~~one of AC power mode and battery power mode~~the power source.

7. (Original) The apparatus of claim 5, wherein the first clock signal has a higher frequency than the second clock signal and the second clock signal has a higher frequency than the third clock signal.

8. (Currently Amended) The apparatus of claim [[4]]1, wherein the ~~second PLL~~ logic device increases ~~the~~ a frequency of the second clock signal in ~~the~~ an AC power mode ~~or~~ and outputs the second clock signal without a frequency adjustment in ~~the~~ a battery power mode.

9. (Currently Amended) The apparatus of claim [[4]]1, wherein the ~~second PLL~~ logic device ~~decreases the frequency of~~ outputs the second clock signal in a battery power mode ~~or outputs the second clock signal~~ without a frequency adjustment ~~in the AC power mode~~.

10. (Currently Amended) The apparatus of claim 6, wherein the ~~third PLL~~ second logic device increases ~~the~~ a frequency of the ~~second~~ third clock signal in ~~the~~ an AC power mode ~~or~~ and outputs the third clock signal without a frequency adjustment in ~~the~~ a battery power mode.

11. (Currently Amended) The apparatus of claim 6, wherein the ~~third PLL~~ second logic device ~~decreases~~outputs ~~the frequency of~~ the ~~second~~ third clock signal in a battery power mode ~~or outputs the third clock signal~~ without a frequency adjustment ~~in the AC power mode~~.

12. (Currently Amended) An apparatus having a CPU and a bridge controller, wherein the improvement comprises:

a clock generator generating a first clock signal; and

a clock adjustor receiving the first clock signal and operating in ~~one of AC power mode or battery power mode~~a power source mode, said clock adjustor generating a second clock signal for the CPU and a third clock signal for the bridge controller, wherein the second and third clock signals are two distinct clock signals outputted by the clock adjustor and have ~~different~~ frequencies that are independent of each other.

13. (Currently Amended) The apparatus of claim 12, wherein the bridge controller controls a clock speed of a bus for data communication among a plurality of peripheral devices of the ~~portable device~~apparatus.

14. (Currently Amended) The apparatus of claim 12, wherein the clock adjustor is a ~~first~~ phase locked loop (PLL).

15. (Currently Amended) The apparatus of claim 12, wherein the ~~improvement~~ CPU further comprises a ~~second~~ phase locked loop (PLL) receiving the second clock signal for the CPU and adjusting the second clock signal based on one of AC power mode and battery power mode.

16. (Currently Amended) The apparatus of claim 12, wherein the ~~portable device~~apparatus further includes a video processor and the clock adjustor generates a fourth

clock signal for the video processor, the fourth clock signal being distinct from the second and third clock signals and having a different frequency than the second and third clock signals.

17. (Original) The apparatus of claim 16, wherein the second clock signal has a higher frequency than the third clock signal and the third clock signal has a higher frequency than the fourth clock signal.

18. (Currently Amended) The apparatus of claim ~~16~~12, wherein the ~~first and fourth clock signals have the same frequency~~power source is one of an AC power mode or a battery power mode.

19. (Currently Amended) A method for ~~optimizing~~ performing clock speed generation, comprising:

receiving a base clock signal;

selectively multiplying the base clock signal by a first factor to produce a first higher frequency clock signal, and by a second factor to produce a second higher frequency clock signal, wherein the first and second higher frequency clock ~~signal is~~signals are different and phase-locked with the base clock signal;

receiving a power mode signal ~~indicating either an AC or a battery source~~; and

selectively outputting the first higher frequency clock signal to a first device ~~when the AC source is indicated, and outputting the base clock signal to the first device when the battery source is indicated~~ and the second higher frequency clock signal to a second device based on the power mode signal.

20. (New) The method of claim 19, wherein the power mode signal is an AC power mode signal or a battery power mode signal and the second higher frequency clock signal is selectively output independent of the first higher frequency clock signal.

21. (New) A method for performing clock speed generation, comprising:

supplying a first clock signal by a first logic to generate a first higher frequency clock signal to a CPU;

supplying a second clock signal by a second logic to generate a second higher frequency clock signal to a bridge controller, wherein the first and second clock signals are distinct;

receiving by the second logic, a power mode signal and adjusting the second clock signal; and

selectively outputting the second higher frequency clock signal based on the power mode signal independent of the first clock signal.

22. (New) The method of claim 21, wherein the first clock signal is greater than the second clock signal.

23. (New) The method of claim 21, wherein the first logic and the second logic are PLLs (Phase Locked Loop).

24. (New) The method of claim 21, wherein the power mode signal is an AC power mode signal or battery power mode signal.

25. (New) The apparatus of claims 6, wherein the first logic is a phase locked loop (PLL) and the second logic device is a PLL.